REMARKS

The Examiner's Action mailed on February 5, 2009, has been received and its contents carefully considered.

In this Amendment, Applicants have amended claims 1, 6 and 8. Claims 1 and 8 are the independent claims, and claims 1-3, 5-9, 11-13, 15-17, 19 and 20 remain pending and under consideration in the application, claims 4, 10, 14 and 18 having been withdrawn. For at least the following reasons, it is submitted that this application is in condition for allowance.

FIG. 5 was objected to, and has accordingly been amended by replacement sheet submitted herewith to show the legend 'Prior Art'. It is therefore respectfully requested that this objection be withdrawn.

Claims 1-3, 5-9, 11-13, 15-17, 19 and 20 were rejected under 35 U.S.C. §103(a) as being obvious over *Saitoh et al.* (U.S. 2002/0185705 A1) in view of *Saito et al.* (U.S. 2002/0005549 A1). This rejection is respectfully traversed.

Claims 1 and 8 as amended now recite that "a part of the filling material is located in the semiconductor substrate", which is supported by FIG. 1, 2(c), 3, 4(c) and 5 and the related descriptions in the present application.

For example, see ¶[0048], describing FIG. 1:

> **[0001]** Inside the respective trenches **4**, silicon oxide portions **15** are provided in bottoms of the trenches **4**, and polysilicon portions **16** are provided on the silicon oxide portions **15**. Silicon oxide films **5** are respectively present between the trenches **4** and the polysilicon portions **16**. The trenches **4** are each almost

completely filled with the silicon oxide portion **15** and the polysilicon portion **16**. Thus, the silicon substrate **2** is less liable to be warped.

In this non-limiting example of the present invention, it can be seen in FIG. 1 that the trenches **4** penetrate into the substrate **2**, and therefore part of the Silicon Oxide portion **15** of the filling material is "located in the semiconductor substrate".

The Office Action apparently regards layer **11** in Figs. 8, 10A and the like of *Saitoh et al.* as corresponding to the semiconductor substrate in the present invention. However, layer **11** of *Saitoh et al.* is named as a "first drift layer" and therefore is comparable to the drift layer in the present invention.

A layer located lower than the first drift layer **11** (for example, the drain layer **10**) of *Saitoh et al.* would be comparable to the semiconductor substrate in the present invention. Therefore, the trench **24** of *Saitoh et al.* does not reach the semiconductor substrate and the insulating layer **22** filled in the trench **24** is not located in the semiconductor substrate.

Consequently, *Saitoh et al.* does not teach or suggest that "a part of the filling material is located in the semiconductor substrate" as recited in claims 1 and 8.

¶¶[0137]-[0140] and [0198] of the *Saito et al.* reference were also asserted in this rejection, and read as follows:

[0137] (Ninth Embodiment)

[0138] FIG. 13 is a sectional view of the element structure of a vertical power MOSFET according to a ninth embodiment of the present invention. Since the configuration of a MOSFET is the same as that of FIG. 1 or FIG. 9 except for the buried layers, repetitive explanation will be omitted and only the characteristic part will be explained.

[0139] In the n^- drift layers **2** under the gate electrodes **6**, trenches **32** are made. In each trench **32**, a buried layer **8b** made of a silicon oxide layer and a polysilicon layer **18b** with a U-shaped cross section are buried alternately. The polysilicon layer **18b** is connected electrically to the n^- drift layers **2**. The silicon oxide layer **8b** to become a buried layer is also shaped like almost the letter U.

[0140] When the MOSFET is off, electrons flow from the n^- drift layer **2** to the polysilicon layer **18b** and are trapped there, thereby dividing the electric field in the n^- drift layer **2**, which improves the breakdown voltage of the MOSFET. In this structure, since the trench is formed by depositing the oxide layer **8b** and polysilicon layer **18b** without performing epitaxial growth for burying, great cost reduction can be expected.

[0198] In the eleventh to seventeenth embodiments, examples of burying a plurality of buried layers in a drift layer have been explained as means for solving the tradeoff between the on-resistance and breakdown voltage of a power semiconductor device. The tradeoff solving means is not limited to buried layers. Use of vertical Resurf layers produces a similar effect. The following is an explanation of such embodiments.

The Office Action cites FIG. 13 and the above paragraphs of *Saito et al.* with respect to the upper surface of the filling material and with respect to the RESURF layer. However, nothing therein discloses that "a part of the filling material is located in the semiconductor substrate". As noted in ¶[0138] reproduced above, the omitted reference numbers in the above description of FIG. 13 can be found, e.g. in ¶[0048] describing FIG. 1:

[0048] On an n^+ silicon substrate **1**, an n^- drift layer **2** is formed. At the surface of the n^- drift layer **2**, a p^- well layer **3** is selectively formed. At the surface of the p^- well layer **3**, n^+ source layers **4** are selectively formed. Above the n^+ source layers **4** and n^- drift layer **2**, gate electrodes **6** are formed via a gate insulating film **5**. A source electrode **7** is formed on the p^- well layer **3** and n^+ source layer **4** in such a manner

> that the electrode **7** connects to the p^- well layer **3** and n^+ source layers **4**. In the n^- drift layer **2**, a plurality of buried layers **8** are buried. On the bottom surface of the n^+ silicon substrate **1**, a drain electrode **9** is provided. In this structure, carriers are trapped in the buried layers **8**, thereby dividing an electric field in the n^- drift layer **2** as shown in FIG. 2. Consequently, even when the dopant concentration of the n^- drift layer **2** is raised to decrease the on-resistance, the original breakdown voltage can be maintained, which enables a low on-resistance exceeding the limit to be realized.

Therefore, with reference to the above, it can be seen in FIG. 13 of *Saito et al.*, that trenches **32** are filled by a buried layer **8b** made of a silicon oxide layer and by a polysilicon layer **18b**, and that this filling material penetrates only into the n^- drift layer **2**, and not into the n^+ silicon substrate **1**.

Hence, neither *Saitoh et al.* nor *Saito et al.*, whether taken separately or in combination, teaches or suggests trenches in which "a part of the filling material is located in the semiconductor substrate" as recited in claims 1 and 8, which are therefore allowable, together with claims 2, 3, 5-7, 9, 11-13, 15-17, 19 and 20 that depend therefrom.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

No remittance is believed to be due. Should any fee be required, however, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,

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Date

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